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TTN

In re Patent Application of:
MEARS
Serial No. not yet assigned
Filed: **herewith**
Attorney Docket: **62601_CON1**

THIS APPLICATION IS A CONTINUATION IN
PART OF 10/647,060 FILED 8/22/2003
WHICH IS A CIP OF 10/603,696
06/26/2003 WHICH WHICH IS A
CIP OF 10/603,621 06/26/2003

IN THE SPECIFICATION:

Please replace the paragraph 0001, with the following rewritten paragraph:

This application is a continuation of 10/647,060 filed 8/22/03, which is a continuation-in-part of U.S. Patent Applications Serial Nos. 10/603,696 and 10/603,621 filed on June 26, 2003, the entire disclosures of which are incorporated by reference herein.

Please replace the paragraph 0056, with the following rewritten paragraph:

FIG. 6E depicts the devices after the gate oxide layers **416** and the gates **418** are formed. To form these layers, a thin gate oxide is deposited, and steps of poly deposition, patterning, and etching are performed. Poly deposition refers to low pressure chemical vapor deposition (LPCVD) of silicon onto an oxide (hence it forms a polycrystalline material). The step includes doping with P+ or As- to make it conducting and the layer is around 250 nm thick.

Please replace the paragraph 0058, with the following rewritten paragraph:

In FIG. 6F, lowly doped source and drain regions **420, 422** are formed adjacent the channels 424 and 426. These regions are formed using n-type and p-type LDD implantation, annealing, and cleaning. "LDD" refers to n-type lowly doped drain, or on the source side, p-type lowly doped source. This is a low energy/low dose implant that is the same ion type as